Optimum Power and Ground Bump Pad and Bump Patterns for Flip Chip Packaging

[001] This invention relates to the power and ground bumps on flip chips and bump pads on substrates for the mounting of flip chips thereon, and in particular is concerned with optimizing the power and ground bump and bump pad patterns to provide improved routing and electrical performance.

Background of the Invention

[002] In the conventional technology for PCB substrate manufacture, the substrate having multiple layers, mechanical drilling was employed to produce vias extending through all layers. The chip has a pattern of bumps formed on its surface, for connection to bump pads on the substrate. The bumps were normally in either orthogonal or staggered patterns. The chips were positioned on the substrate as desired. The circuits on the various layers of the substrate are then designed only to connect to the appropriate vias. Thus, in a four-layer substrate, the top and bottom layers were usually signal planes and the two middle layers were power and ground planes, respectively.

[003] A more recent technology is to use microvias which connect only two adjacent layers. With this technology, the location of the power and ground bump pads on a die will influence the routing and electrical performance of the substrate. The present non-selective positioning of power and ground bump pads on the substrate prevents obtaining optimum routing and electrical performances.

Description of the Invention

[004] In a PCB substrate, as used for flip chip assemblies or packaging, there are several layers, with two of the layers reserved for power and ground planes respectively. The positioning of power and ground bumps on the chip are normally in a predetermined location. The layers are interconnected by vias and previously the vias were produced by through drilling to provide connections to all layers. The circuit patterns on the various layers, or planes, are arranged such that connection occurs at the appropriate vias to connect to appropriate bump pads and bumps.

By using microvias, interconnecting only two adjacent layers, the positioning of the chip power and ground bumps influences routing density and electrical performance. By designating appropriate patterning of the bump pads on the substrate, improved routing and electrical performance is obtained.

[005] Thus, with the present invention, a substrate, for flip chip packaging, has a plurality of layers, providing a power plane, a ground plane and at least one signal plane. Power, ground and signal bump pads are formed on one surface of the substrate, for example, the top surface. The power and ground bump pads extend in rows across the substrate at designated positions. Microvias at the designated positions connect the power bump pads and ground bump pads respectively to the power and ground planes. Further microvias connect signal bump pads directly to a signal plane. On the flip chip power and ground pads extend in parallel rows in a designated position, to match the rows of power and ground bump pads.

Brief Description of the Drawings

[006] Figure 1 is a cross-section through a four-layer substrate, illustrating through layer connections with drilled vias in a conventional PCB structure;

[007] Figure 2 is a cross-section through a four-layer substrate, illustrating the more recent microvias connecting only two adjacent layers; and with non-designated bumps and bump pad locations;

[008] Figure 3 is a cross-section through a four-layer substrate, having a designated bump and bump pad patterns, with appropriate microvia connections;

[009] Figures 4(a) and 4(b) illustrate, in plan view, two bump patterns on a flip chip, in accordance with the invention.

Detailed Description of the Drawings

[0010] Figure 1 illustrates the interconnection through a four-layer substrate or PCB, indicated generally at 20. The four layers are indicated at 22, 24, 26 and 28. Normally the power and ground planes are the second and third layers 24 and 26. The first and fourth layers form the signal layers.

[0011] In a conventional printed circuit board, all the layers are interconnected by drilled vias 36 which extend through to all layers. Flip chip bump pads 38 extend on the first layer 22 at the end of each via, providing connection thereto. With this arrangement, there are no designated chip bump or bump pads specific for ground, power or signal.

[0012] The circuit patterns both on the chip and the substrate are such that certain bumps and bump pads cooperate to provide the desired connection between flip chip and substrate. The pattern of bumps on the flip chip and bump pads on the substrate are not in any designated form. Thus there is no designated pattern for the ground and power bumps and bump pads. This is not of any consequence with through vias as in Figure 1. The positioning of related bumps and bump pads is dependent upon the chip circuitry and associated substrate circuitry.

[0013] In printed circuit boards with microvias, for optimum routing and electrical performance it is necessary to position the chip bumps for power and ground bumps at specific positions. Without this, optimum results are not obtained. Thus, as seen in Figure 2 for example, because of the positioning of the power and ground bump pads 50 and 52 and signal pads 54, direct connection between a pad and the required plane does not occur. Some of the signals need to go to the second layer and back to the first layer through microvias. Routing will be more difficult and electrical performance less than optimum as there is no power or ground plane for those signals to refer to.

[0014] Ideally, it is desirable that connections from a bump pad to a plane be made in as direct a manner as possible. Figure 3 illustrates one such arrangement. In this arrangement, the first and second rows of flip chip bumps, signal bumps, will connect to the first and second rows of bump pads 60, which in turn connect to the first layer 22, having a signal plane. The next two rows of bump pads are power and ground bump pads 62 and 64 respectively, the ground bump pads being connected directly to the ground plane at the second layer 24 and the power bump pads connected directly to the power plane at the third layer 26, by microvias 66. It will be seen that the rows of power and ground bump pads, 62 and 64, and the signal bump pads 60, are in sequence, to match the positioning of the signal, power and ground planes 22, 24 and 26. This is the desirable arrangement. Further rows of signal bump pads connect via microvias 66 directly to the signal plane at the fourth layer. It will be seen that it is not necessary to provide for

connections back through layers, as occurs in Figure 2. Thus routing is improved and electrical performance improved.

[0015] The bumps on the flip chip are similarly designated. This is illustrated in Figures 4(a) and 4(b). Chip bumps are normally arranged either in an orthogonal pattern, as in Figure 4(a) or in a staggered pattern, as in Figure 4(b). Whereas in the previous arrangements with through vias, no particular pattern of power and ground bumps occurred in the present invention the power and ground bumps extend in two adjacent parallel rows – row 70 for power for example, with bumps 72 and now 74 for ground with bumps 76. Signal bumps 78 are also provided.

[0016] The power and ground bumps 72, 76 are positioned to connect to the power and ground bump pads 62 and 64 on the substrate and thus directly to the power and ground planes by the microvias 66.

[0017] Thus, it is arranged that the ground and power bumps on the chip and bump pads on the substrate are in designated rows on the chip and on the substrate so as to form cooperating connections. Microvias are formed in the substrate to provide direct connection to the respective ground and power planes. The signal bumps on the flip chip, connect directly to one signal plane or via microvias directly to the other signal plane.

[0018] The circuit diagrams for the various planes are designed so that appropriate connections are made to the microvias and thus to the appropriate bump pads.

[0019] Often, in electronic component design, computers are used to automate much of the design process. For example, computers automatically route interconnects within a package or an integrated circuit, within a board for use in a hybrid circuit or within a printed circuit board for other applications. The use of computers allows for repeatable use of templates, automated routing, automated transfer of programming data to a manufacturing system, repeatable production results, automated parts lists for PCB manufacturing, and so forth. This highly automated approach to design is considered desirable.

[0020] The present invention is also implementable on a computer or other processing system. A program is typically delivered stored on a non-volatile storage medium such as a CD-ROM, a DVD-ROM, a floppy disk, etc. The program is input to the computer system in a

process typically referred to as installation. Once installed, the program is executed. According to the present invention, execution of the program results in programming for the manufacturing process for forming a flip chip package in accordance with the above description. Alternatively, execution of the program provides a template that results in programming for the manufacturing process for forming in a flip chip package in accordance with the above description.

[0021] Of course, when the computer is coupled with a manufacturing system, execution of the program results in the actual flip chip package since the program provides instructions to the manufacturing system for forming the package. As such, many embodiments of the invention may be envisioned for forming a flip chip package, a representation of same for use in manufacturing, or for providing a template of a representation of same for use in manufacturing.

[0022] It is possible to provide some other arrangement of the various planes, in which case the relative positioning of power and ground bump pads is such as to provide the direct connection to the power and ground planes.